

Transistor model is not critical and different models may be mixed as long as they are the right NPN/PNP type, but parameters should match: ... as marked  
 \* within any three-transistor/mirror/multiplier  
 \* between each output driver transistor and the corresponding NPN/PNP "compensation" transistor  
 Also, beware of different pinouts!

#### Optional JFET modification:

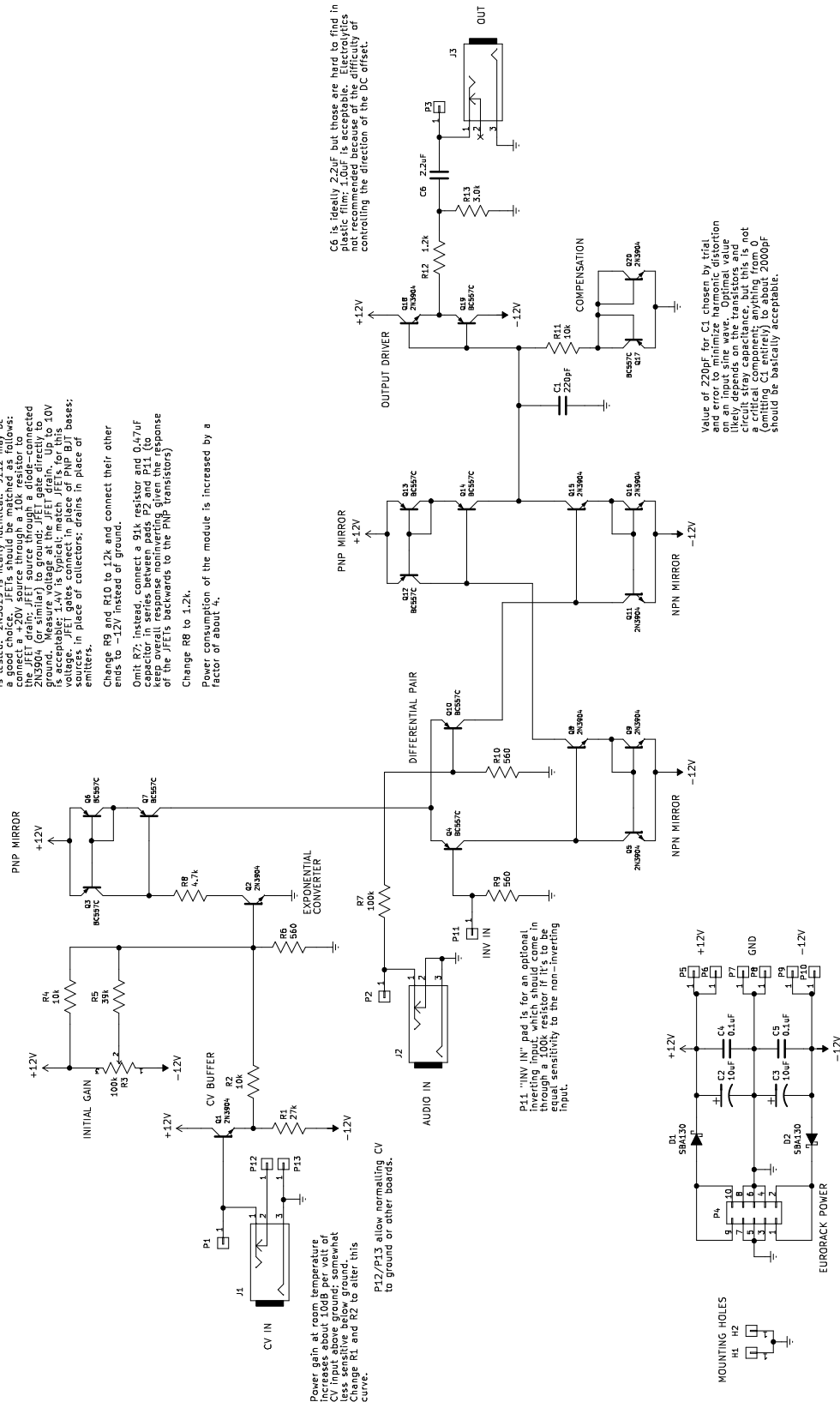
Replace Q4 and Q10 by N-channel JFETs, Type MPF102 is tested. 2N3815 is nearly identical. R12 may be omitted and the JFET gates connected to ground. Connect a +20V source through a 10k resistor to the JFET drain; JFET source through a 10k resistor to ground. Measure voltage at the JFET drain. Up to 10V is acceptable; 1.4V is typical; match JFETs for this voltage. JFET gates connect in place of PNP BJT bases; JFET sources connect in place of PNP BJTs emitters.

Change R9 and R10 to 12k and connect their other ends to -12V instead of ground.

Omit R7; instead, connect a 91k resistor and 0.47uF capacitor in parallel between the JFET gates. This will keep overall response noninverting given the response of the JFETs backwards to the PNP transistors)

Change R8 to 1.2k.

Power consumption of the module is increased by a factor of about 4.



C6 is ideally 2.2uF but those are hard to find in plastic film; 1.0uF is acceptable. Electrolytics are acceptable but they may have an effect on controlling the direction of the DC offset.

Value of 220pF for C1 chosen by trial and error to minimize harmonic distortion and to keep the response time as fast as possible. The value of C1 is likely to depend on the transistors used and circuit stray capacitance, but this is not a critical component; anything from 0 to 1000pF should be basically acceptable.

## MSK 006 EXPONENTIAL VCA

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